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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/657,121	09/07/2000	Randal Craig Swanberg	AUS9-1999-0305-US1	2398

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EXAMINER
PARTHASARATHY, PRAMILA

ART UNIT	PAPER NUMBER
2136	

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DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/657,121	SWANBERG ET AL.	
	Examiner	Art Unit	
	Pramila Parthasarathy	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6,9-14,16-21 and 23-31* is/are allowed.

6)☒ Claim(s) *33-36* is/are rejected.

7)☒ Claim(s) *7,8,15,22 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed on June 21, 2004. The original application contained claims 1 – 36. No claims were cancelled. Claims 1 – 4 and Claim 24 were amended. Presently pending claims are 1- 36.

Claim Objections

2. Claims 15, 22 and 30 are objected to because of the following informalities: Replace "said processor stacks" with "said processor stack is " on line 3 of each claim.

Appropriate correction is required.

Response to Amendment

3. Applicant's arguments filed on June 21, 2004 have been fully considered and found persuasive for the Claims 1 – 6, 9 – 14, 16 – 21 and 23 – 31 but not found persuasive for the Claims 7, 8, 15, 22, 32 – 36 because of the following reasons.

Regarding Claims 1 – 6, 9 – 14, 16 – 21 and 23 – 31, the present invention pertains generally to new memory protection classification specific for stack memory and, more particularly a method and system for stack memory protection. The claimed invention (Claim 1 as representative) recites features such as: " ... generating

new memory page attributes for a page table used to manage memory, each of said new memory page attributes identifying a block of memory as a new class of memory, each of said new memory page attributes generated by a corresponding new load/store instruction; assigning, by an operating system or a processor, a selected one of said new memory page attributes to a selected block of memory, said selected block of memory used as a new class or memory corresponding to said selected new memory page attribute; blocking normal load/stores to a memory block with one of said new memory page attributes; and blocking a first new load/store to a memory block with one of said new memory page attributes not corresponding to said first new load/store."

The prior arts of record teach the concept of memory protection via segment descriptors and process privilege rings; Kane et al. (U.S. Patent Number 5,596,739) is one example of such prior arts. The prior arts of record, however, fail to teach singly or in combination, additionally assigning a new attribute to a selected block of memory thereby creating a new class of memory accessible only by new in load/store instructions, wherein normal load/store instructions are blocked from the block of memory without the assigned new attribute. The examiner agrees with the Applicants arguments with regard to this feature in view of the arts of record; therefore, Examiner favors the allowance of Claims 1 – 6, 9 – 14, 16 – 21 and 23 – 31.

Regarding dependent Claims 7, 15, 22 and 32, the applicant argues that the added limitation "the first memory stack used by a processor to load and store hardware register contents during program execution" so that the OS no longer needs to allocate

specific space in memory as stack memory and likewise does not have to estimate how much memory is needed for program stacks and processor stacks. This argument is not found persuasive as claims do not further narrow the claims 5, 13, 20 and 28 which disclose stack memory with corresponding to the first load/store (program execution) and the generation of error condition whenever a stack memory load/store for a first memory stack is attempted to a second memory stack.

Regarding dependent Claim 8, it is objected as it depends on objected Claim 7.

The Claims 8, 15, 22 and 32, are allowable if they are written in an independent form.

Regarding independent Claim 33, the applicant argues that the cited prior art (CPA) Kane et al. (U.S. Patent Number 5,596,739, hereinafter "Kane") does not teach "partitioning memory device into a plurality of memory spaces on as-needed bases and associating a memory attribute with each memory space; said memory attribute determining a use of each of said memory space". This argument is not found persuasive. Kane discloses the memory control unit segmenting (partitioning) memory into a plurality of memory spaces and assigning privilege levels to the memory space (associating memory attribute with each memory space) so that these memory spaces can be identified with the associated task (Kane Column 1 line 55 – Column 2 line 11 and Column 4 line 57 – Column 5 line 22).

Applicant clearly has failed to explicitly identify specific claim limitations, which would define a patentable distinction over prior arts. Therefore, the examiner respectfully asserts that CPA does teach or suggest the subject matter broadly recited in independent claim 33. Dependent claims 34 – 36 are also rejected at least by virtue of their dependency on independent claims and by other reasons set forth in this office action.

Accordingly, rejections for claims 33 – 36 are respectfully maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 33 – 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Kane et al. (U.S. Patent No: 5,596,739).

Regarding Claim 33, Kane teaches and describes a method of managing a memory device comprising the steps of:

partitioning said memory device into a plurality of memory spaces on an as-needed bases (Column 1 lines 56 – 59); and

associating memory attribute with each memory space; said memory attribute determining a use of each of said memory spaces (Column 1 lines 56 – 59).

Claim 34 is rejected as applied above in rejecting claim 33. Furthermore, Kane teaches and describes a method of managing a memory device, wherein: a particular memory attribute has corresponding load/store instruction (Fig. 1 #114 and Column 2 lines 33 – 37).

Claim 36 is rejected as applied above in rejecting claim 33. Furthermore, Kane teaches and describes a method of managing a memory device, wherein: each of said memory attributes are stored in a memory page table, said memory page table used to manage said memory device (Column 1 lines 64 – 66).

Claim 35 is rejected as applied above in rejecting claim 34. Furthermore, Kane teaches and describes a method of managing a memory device, wherein: a load/store instruction associated with a first memory attribute causes an error condition if attempted on a memory space with a second memory attribute (Column 1 Lines 64 – Column 2 line 8).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pramila Parthasarathy whose telephone number is 571-272-3866. The examiner can normally be reached on 8:00a.m. To 5:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-232-3795.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR only. For more information about the PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pramila Parthasarathy
October 29, 2004.

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100